Edgar Reyes-Rivera

Open to Relocation | Edgar@ReyesRivera.com | ReyesRivera.com
linkedin.com/in/edgar-reyes-rivera | github.com/EdgarReyesRivera

Education

Miami University | GPA: 3.48 — Oxford, OH
Bachelor of Science in Computer Engineering — *Expected May 2027*
Bachelor of Science in Computer Science — *Expected May 2027*

Relevant Coursework: High Performance Computing & Parallel Programming, Computer Organization, Systems I & II, Embedded Systems Design, Digital Systems Design, Comparative Programming Languages, Algorithms I, Data Abstractions & Structures, Network Performance Analysis

Skills & Certifications

Languages: C++, C, CUDA, Python, SystemVerilog, Verilog, RISC-V Assembly, MIPS Assembly, OCaml, Java, SQL

Systems & Performance: GPU Computing, HPC (Slurm), Linux (Arch, Distrobox), Multi-threading, Memory-Mapped I/O, AXI4-Lite, GCC, NVCC

Hardware: FPGA Development, RTL Design, RISC-V Architecture, ARM SoC (Zynq), Digital Circuit Design, I2C, SPI, UART

Tools: Vivado, Quartus, ModelSim, Git, Docker, TrueNAS, Tailscale, MATLAB

Certifications: OASiS Rapid Certification in Semiconductor Manufacturing (University of Cincinnati), including hands-on cleanroom wafer etching

Projects

TinyRV1 RISC-V Processor | *May 2025* — reyesrivera.com/projects/tinyrv1-processor

- Designed and implemented a single-cycle, non-pipelined 32-bit RISC-V processor in Verilog on a DE1-SoC FPGA, executing the eight-instruction TinyRV1 subset (arithmetic, multiply, loads/stores, jumps, branch).
- Built a two-pass Python assembler covering all five RISC-V encoding formats to generate the processor's memory images.
- Verified with self-checking ModelSim testbenches and four on-board test programs; added a single-step mode with live 7-segment register readout.

FPGA-Based Gaussian Blur Image Processing | *Dec 2024* — reyesrivera.com/projects/gaussian-blur-fpga

- Engineered a Gaussian blur filter in Verilog on a Cyclone V (DE1-SoC) FPGA, convolving a 160x120 image with a 3x3 binomial kernel using shift-based fixed-point arithmetic with no hardware divider.
- Designed a custom state machine that filters the image in place in on-chip block RAM in about 4.5 ms per pass (12 cycles per pixel at 50 MHz).
- Drove a 640x480 VGA display at 60 Hz from the same frame memory, upscaling the processed image in hardware.

3D Gaussian Splatting for Radar Imaging *(In Progress)* — reyesrivera.com/projects/radar-gaussian-splatting

- Extending 3D Gaussian Splatting to radar imaging for senior design, reporting findings to Air Force Research Laboratory (AFRL) researchers.
- Evaluating eight radar and splatting codebases on a Slurm-managed Tesla V100 cluster, compiling C++ and CUDA with a pinned CentOS toolchain.
- Building synthetic 3D ground truth: multi-material scenes rendered at known camera poses, to validate with optical 3DGS before radar modeling.

FPGA Network Packet Parser *(In Progress)* — reyesrivera.com/projects/fpga-packet-parser

- Designing a byte-per-clock SystemVerilog state machine that parses UDP-style packet headers and exposes the fields to an ARM core through a hand-written AXI4-Lite register interface on a Zynq SoC.
- Validating against a C++ reference implementation with shared test vectors (valid, malformed, and back-to-back packets) and measuring parsing latency in hardware versus software with cycle counters.

Self-Hosted Homelab Server | *Ongoing*

- Run a TrueNAS Scale server hosting containerized Nextcloud, Pi-hole, Vikunja (daily coursework task board), and CouchDB for Obsidian sync.
- Expose services securely through Tailscale and a Cloudflare Tunnel behind Nginx Proxy Manager, routed through a personal domain.
- Set up remote GPU development: first a GPU in the server for CUDA programs, now a higher-end desktop GPU accessed over SSH.

Experience

RoviSys — Aurora, OH
Software Co-op — *May 2026 – Aug 2026*

- Built full-stack features (C#, .NET, NHibernate, SQL Server, Vue.js, TypeScript) for a client's semiconductor-manufacturing management web app migrated from Visual Basic, tracking process interruptions and tolerances.

Synchrony — Cincinnati, OH
Software Engineer Intern — *Jul 2024 – Sep 2024*

- Researched, prototyped, and presented solutions for internal teams on an agile Enablement Architecture team (Java, JavaScript, React, SQL), iterating on stakeholder feedback before handing findings to the owning teams.

Leadership & Service

President, Society of Hispanic Professional Engineers (SHPE) — *Aug 2025 – May 2026*

- Led a 25-member chapter and its weekly events; served as liaison to National SHPE and the College of Engineering and Computing.
- Managed six corporate sponsor relationships funding member events, including Avery Dennison's recurring $1,000-per-semester sponsorship.